REMARKS/ARGUMENTS

The specification and the claims have been amended as indicated above. Support for the amendment can be found in the specification. No new matter has been added by the amendments. Reconsideration and withdrawal of the rejections are respectfully requested in view of the foregoing amendment and following remarks.

Claims 1-3 and 26-30 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicant traverses the rejection. Support for the feature of "a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region..." is found at least in Fig. 5 and paragraph 43.

Claims 1-3 and 26-30 were rejected under 35 U.S.C. 112, second paragraph. Claim 1 has been amended, so that it does not necessarily require the peripheral junction region to float electrically.

Claims 1-3, 26, 28, and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yano in view of Gross. Applicant traverses the rejection.

The claimed invention relates to power devices that are rated to handle high reverse blocking voltages. Such a power device is provided with a passivation layer made of glass. The glass, however, tends to bend the wafer if the wafer is 6 inches or bigger. See paragraph 28. The use of polymid solves this bending problem, but it decreases the reverse blocking voltage and increase leakage current. The present inventor has discovered that forming the peripheral junction region in the isolation diffusion region solved one or more problems associated with the use of polymid as the passivation layer. See paragraph 32.

As the Examiner correctly noted, Yano does not disclose or suggest "a peripheral junction region of second conductivity," in the manner recited. Gross does not remedy the deficiency of Yano, contrary to the Examiner's assertion. Yano, like the claimed invention, relates to a power device. Gross relates to forming resistors in isolation regions of the integrated circuits. The peripheral junction region of claim 1 is not a resistor. Gross does not provide any suggestion or motivation as to why "the peripheral junction region" should be provided in the element isolation region 17 of Yano. Accordingly, neither Yano nor Gross provide any

motivation or suggestion for the "peripheral junction region," in the manner recited. Claim 1 is allowable.

Claim 2 depends from claim 1 and is allowable at least for this reason. In addition, claim 2 recites, "the peripheral junction region is a P+ region and the isolation diffusion region is a P region." Gross discloses forming a P-type resistor in the N-type region (see Fig. 2) and an N-type resistor in the P-type region (see Fig. 3). Gross does not disclose the features recited in claim 2.

Claim 3 depends from claim 1 and is allowable at least for this reason. In addition, claim 3 recites, "the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region." Neither Yano nor Gross disclose or suggest this feature.

Claim 26 depends from claim 1 and is allowable at least for this reason. In addition, claim 26 recites, "the passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region. Neither Yano nor Gross disclose or suggest this feature.

Claim 28 depends from claim 1 and is allowable at least for this reason. In addition, claim 28 recites, "the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region."

Claims 27 and 29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yano and Gross and further in view of Collins. Claims 27 and 29 depend from claim 1 are allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 206-467-9600.

Respectfully submitted,

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